WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

an information storing part for storing an m-bit information code and an n-bit check code for one piece of position information;

an ECC circuit capable of correcting, from an information code and a check code stored in said information storing part, an error of said information code to x bits; and

a parallel test circuit for receiving an information code and a check code for test with the same bits stored in said information storing part and deciding a defect with said x+1 bits or more for one piece of position information as being defective.

2. The semiconductor memory device according to claim 1,

wherein a plurality of said information storing parts are accessible individually,

wherein a plurality of said parallel test circuits are provided corresponding to said plurality of information storing parts, respectively,

wherein said ECC circuit is provided to be shared among said plurality of information storing parts, and

wherein said plurality of information storing parts store an information code and a check code for test in the same pattern, said plurality of parallel test circuits are valid in parallel in test mode, each deciding a defect with said x+1 bits or more

as being defective for outputting individually.

3. The semiconductor memory device according to claim 1, further comprising:

a z-bit information input/output terminal in which the relation of z > n is established; and

a write signal path in which at information input in test mode, an information input terminal with n bits of z bits is used to be written as an n-bit check code into said information storing part and an information input/output terminal with the remaining z-n bits or less is used to be written thereinto as an information code of said information storing part.

4. The semiconductor memory device according to claim 3, further comprising a read path in which an information code and a check code stored in said information storing part are used for reading in test mode corresponding to allocation of said information code and check code to the information input/output terminal, used at said information input in test mode.

5. A semiconductor memory device comprising:

an information storing part for storing an m-bit information code and an n-bit check code for one piece of position information; and

an ECC circuit capable of correcting, from an information code and a check code stored in said information storing part, an error of said information code to x bits,

wherein in said information storing part with reference to said ECC circuit, the storing location of said information code is allocated to the position capable of inputting and outputting information faster than the storing location of said check code.

6. A test method of a semiconductor memory device including:

an information storing part for storing an m-bit information code and an n-bit check code for one piece of position information;

an ECC circuit capable of correcting, from an information code and a check code stored in said information storing part, an error of said information code to x bits;

and a test circuit for receiving an information code and a check code stored in said information storing part,

wherein an information code and a check code for test with the same bits are stored in said information storing part, said stored information code and check code for test are transmitted to said test circuit, and a defect with said x+1 bits or more for one piece of position information is decided as being defective.

7. The test method of a semiconductor memory device according to claim 6,

wherein said semiconductor memory device includes:

a plurality of information storing parts accessible individually;

a plurality of test circuits corresponding to said plurality of information storing parts, respectively; and

an ECC circuit provided to be shared corresponding to said plurality of information storing parts,

wherein said plurality of information storing parts store an information code and a check code for test in the same pattern, and said plurality of test circuits are valid in parallel in test mode, each deciding a defect with said x+1 bits or more as being defective for outputting individually.

8. The test method of a semiconductor memory device according to claim 6,

wherein said semiconductor memory device includes a z-bit information input/output terminal in which the relation of z > n is established,

wherein at information input in test mode, an information input terminal with n bits of said z bits is used to be written as an n-bit check code into said information storing part and an information input/output terminal with the remaining z-n bits or less is used to be written thereinto as an information code of said information storing part.

9. The test method of a semiconductor memory device according to claim 8,

wherein an information code and a check code stored in said information storing part are used for reading in test mode corresponding to allocation of said information code and check

code to the information input/output terminal, used at said information input in test mode.